EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	799	438/455,458.ccls. and epitaxial$2	US-PGPUB; USPAT	OR	ON	2007/09/25 13:31
L2	501	1 and @ad<"20030908"	US-PGPUB; USPAT	OR	ON	2007/09/25 13:30
L3	196	2 and ((implant$5 or dop$3) with hydrogen)	US-PGPUB; USPAT	OR	ON	2007/09/25 13:31
L4	29	3 and (boron with epitaxial$2)	US-PGPUB; USPAT	OR	ON	2007/09/25 13:32
L5	37	(epitaxial$2 with boron) and (hydrogen with (dop$3 or implant$5))	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/25 13:49
S1	1033	smart near3 cut	US-PGPUB; USPAT	OR	ON	2007/09/25 09:24
S2	574	S1 and ((implant$5 or dop$3) with hydrogen)	US-PGPUB; USPAT	OR	ON	2007/09/25 13:31
S3	350	S2 and epitaxial$2	US-PGPUB; USPAT	OR	ON	2007/09/25 13:48
S4	177	S3 and @ad<"20030908"	US-PGPUB; USPAT	OR	ON	2007/09/25 13:30
S5	20	S4 and (boron same epitaxial$3)	US-PGPUB; USPAT	OR	ON	2007/09/25 10:34
S6	11535	((implant$5 or dop$3) with hydrogen)	US-PGPUB; USPAT	OR	ON	2007/09/25 11:41
S7	290	S6 and (epitaxial$2 with boron)	US-PGPUB; USPAT	OR	ON	2007/09/25 11:41
S8	213	S7 and @ad<"20030908"	US-PGPUB; USPAT	OR	ON	2007/09/25 11:42
S9	207	S8 not S4	US-PGPUB; USPAT	OR	ON	2007/09/25 13:18

US-PAT-NO: 5882987

DOCUMENT-IDENTIFIER: US 5882987 A

TITLE: Smart-cut process for the production of thin semiconductor material films

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Brief Summary Text - BSTX (18):

In the present invention, a thin semiconductor layer of substantially uniform thickness upon which semiconductor structures can be subsequently formed is fabricated by providing a first wafer comprising a semiconductor substrate (hereinafter referred to as a silicon (Si) substrate); forming an etch stop layer upon the first wafer; forming an **epitaxial** device layer on the etch stop layer; forming a bonding layer on the device layer; implanting ions into the silicon substrate in order to form a buried layer therein; bonding the bonding layer to a second wafer; heating the bonded first and second wafers; separating the bonded first and second wafers along the buried layer so that the second wafer has a top surface layer comprising Si from the first wafer; and removing the top surface layer and the etch stop layer, whereby underlying portions of the **epitaxial** device layer remain on the second wafer to form the thin semiconductor layer.

Brief Summary Text - BSTX (19):

Another embodiment within the scope of this invention includes etching the top surface layer in a first etchant which does not appreciably attack the etch stop layer, and then etching the etch stop layer in a second etchant which does not appreciably attack a remaining part of the **epitaxial** device layer.

Brief Summary Text - BSTX (20):

A further embodiment within the scope of this invention includes photolithographically patterning and etching the bonding layer and the **epitaxial** device layer to form apertures therein after the step of implanting ions.

Detailed Description Text - DETX (3):

FIG. 4 is a flow diagram of one exemplary embodiment of a fabrication process in accordance with the present invention. FIGS. 5A to 5G show the corresponding cross-sections of selected steps from the process flow diagram of

FIG. 4. A single crystalline semiconductor wafer 500, preferably a silicon substrate, having a desired orientation is used as the starting point at step 400. The wafer 500 does not have to be device quality because no part of the starting wafer 500 ends up in the final SOI structure. The wafer 500 typically has a low dopant concentration in the range of 10.sup.15 to 10.sup.18 impurities/cm.sup.3. A thin etch stop layer 505 having a predetermined composition and thickness is **epitaxially** grown over the wafer surface. The etch stop layer 505 has a preferred thickness in the range of about 3.9.times.10.sup.-7 to 7.8.times.10.sup.-5 inch (100 to 2000 .ANG.), with the most preferred thickness being about 9.8.times.10.sup.-7 inch (250 .ANG.). The etch stop material is chosen so that it is selective in its etch behavior as compared to the substrate material. For example, a high doped (p+or n+) silicon layer, a silicon-germanium (Si-Ge) layer, a strained Si-Ge layer, or a Ge layer can be used as an etch stop layer. Preferably, the etch stop layer 505 is a high doped Ge compensated layer of Si-Ge. The dopant concentration is preferably in the range between 10.sup.20 and 10.sup.21 atoms/cm.sup.3 of **boron**. This layer is preferably deposited using a chemical vapor deposition (CVD) process.

Detailed Description Text - DETX (4):

A thin device layer 510 having a selected thickness and dopant concentration is then **epitaxially** deposited over the etch stop layer 505, as shown in FIG. 5A. The choice of etch stop layer 505 should take into account strain mismatch between etch stop layer 505 and device layer 510, so that a good quality low dislocation device layer 510 can be deposited. The device layer 510 can be Si, Si-Ge, Ge, or any other compound semiconductor. Si-Ge layers used in this application may contain 5 to 30 atomic percent Ge. The thickness of the device layer 510 is preferably about 3.9.times.10.sup.-6 inch (1000 .ANG.) and can range from about 2.times.10.sup.-6 to 2.times.10.sup.-5 inch (500 to 5000 .ANG.), depending on the application needs of the device.

DOCUMENT-IDENTIFIER: US 20010029072 A1

TITLE: Method of recycling a delaminated wafer and a silicon wafer used for the recycling

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Abstract Paragraph - ABTX (1):

There is disclosed a method of recycling a delaminated wafer produced as a by-product in producing an SOI wafer according to a hydrogen ion delaminating method by reprocessing it for reuse as a silicon wafer, wherein at least polishing of the delaminated wafer for removing of a step in the peripheral part of the delaminated wafer and heat treatment in a reducing atmosphere containing hydrogen are conducted as the reprocessing. There are provided a method of appropriately reprocessing a delaminated wafer produced as a by-product in a hydrogen ion delaminating method to reuse it as a silicon wafer actually, and particularly, a method of reprocessing an expensive wafer such as an **epitaxial** wafer many times for reuse, to improve productivity of SOI wafer having a high quality SOI layer, and to reduce producing cost.

Application Filing Date - APD (1):

20010605

Summary of Invention Paragraph - BSTX (3):

[0002] The present invention relates to a method of recycling a silicon wafer by reprocessing a delaminated (split) wafer produced as a by-product in a **hydrogen** ion delaminating method (also called a **smart cut** method) wherein an ion-**implanted** wafer is bonded to another wafer and a portion of the ion-**implanted** wafer is delaminated to thereby obtain an SOI (silicon on insulator) wafer. Particularly, the present invention relates to a method of reprocessing the delaminated wafer many times, and reusing it many times.

Summary of Invention Paragraph - BSTX (10):

[0009] To solve the problem, there is proposed, for example, a method wherein CZ wafer on which an **epitaxial** layer is grown is bonded to other wafer on the side of the **epitaxial** layer, and the silicon wafer which constitutes a base is ground and polished to form a SOI layer (see Japanese Patent Application Laid-open (Kokai) No. 7-254689). According to the method, the above mentioned crystal defects such as COP can be surely eliminated. However, since it is necessary to use an expensive **epitaxial** wafer, production cost of

the SOI wafer gets far higher.

Summary of Invention Paragraph - BSTX (13):

[0012] Recently, public attention has been drawn to a new method of fabricating an SOI wafer in which an ion-**implanted** wafer is bonded to another wafer and a portion of the ion-**implanted** wafer is delaminated (split) to thereby obtain an SOI wafer (**hydrogen** ion delaminating method: so-called **smart-cut** method). In this method, an oxide film is formed on the surface of at least one of two silicon wafers; and **hydrogen** ions or rare gas ions are **implanted** into the surface of one of the two silicon wafers in order to form a fine bubble layer (enclosed layer) within the wafer; the ion-**implanted** silicon wafer is superposed on the other silicon wafer such that the ion-**implanted** surface comes into close contact with the surface of the other silicon wafer via the oxide film; heat treatment is performed to delaminate a portion of the ion-**implanted** wafer while the fine bubble layer is used as a delaminating plane, in order to form a thin film; and heat treatment (bonding heat treatment) is further performed to firmly bond the thin film and the other wafer, to thereby obtain an SOI wafer (see Japanese Patent Application Laid-Open (kokai) No. 5-211128 or U.S. Pat. No. 5,374,564). Also, in this method, since the surface formed as a result of delamination is a good mirror-like surface, an SOI wafer whose SOI layer has a high thickness uniformity is obtained with relative ease.

Summary of Invention Paragraph - BSTX (14):

[0013] Also in the **hydrogen** ion delaminating method described above, not only silicon wafers are bonded together, but also an ion-**implanted** silicon wafer may be bonded directly to an insulator wafer of SiO.sub.2, SiC, Al.sub.2O.sub.3, etc., in order to form an SOI layer.

Summary of Invention Paragraph - BSTX (17):

[0016] In this case, it may be conceived that the surface of the delaminated wafer is ground, and then polished in order to remove the step in the peripheral part and the damage layer, and to improve surface roughness or the like. However, in order to improve the surface properties by grinding and polishing, long processing time and a lot of stock removal are required. Moreover, in the case that an **epitaxial** layer is used as a bond wafer in the hydrogen ion delimitation method, and SOI layer is made of an **epitaxial** layer, since the **epitaxial** layer remaining on the delaminated layer is completely removed, the **epitaxial** layer cannot be reused as a SOI layer. Accordingly, cost for fabrication of SOI wafer cannot be reduced.

Summary of Invention Paragraph - BSTX (20):

[0018] The present invention has been accomplished to solve the above-mentioned problems, and an object of the present invention is to provide a method of appropriately reprocessing a delaminated wafer produced as a by-product in a hydrogen ion delaminating method to reuse it as a silicon wafer actually. Particularly, the object of the present invention is to provide a method of reprocessing an expensive wafer such as an **epitaxial** wafer many times for reuse, to improve productivity of SOI wafer having a high quality SOI layer, and to reduce producing cost.

Summary of Invention Paragraph - BSTX (24):

[0022] The present invention also provides a method of recycling a delaminated wafer produced as a by-product in producing an SOI wafer according to a hydrogen ion delaminating method in which an **epitaxial** wafer is used as a bond wafer by reprocessing it for reuse as a silicon wafer wherein polishing of the delaminated wafer for removal of a step in the peripheral part of the delaminated wafer and heat treatment in a reducing atmosphere containing hydrogen are at least conducted as the reprocessing.

Summary of Invention Paragraph - BSTX (25):

[0023] As described above, since the stock removal is kept to a minimum to reprocess the delaminated wafer in the method of the present invention, the **epitaxial** layer of the expensive **epitaxial** wafer can be reprocessed and reused many times, so that the SOI wafer of high quality can be fabricated at low cost.

Summary of Invention Paragraph - BSTX (33):

[0031] With such a small stock removal, the peripheral step can be surely removed. Furthermore, since the stock removal is small, the **epitaxial** layer can be used as the SOI layer many times by reprocessing the delaminated wafer, even when the **epitaxial** wafer is used as a bond wafer.

Summary of Invention Paragraph - BSTX (44):

[0042] As described above, when the delaminated wafer produced as a by-product in the hydrogen ion delaminating method is reprocessed appropriately according to the present invention, it can be actually reused as a silicon wafer. Particularly, the stock removal of the delaminated wafer can be decreased, an expensive wafer such as an **epitaxial** wafer can be reprocessed many times to be reused many times. Thereby, improvement in productivity of the SOI wafer having the SOI layer of high quality and cost reduction can be achieved.

Detail Description Paragraph - DETX (4):

[0054] In step (a) of the hydrogen ion delaminating method shown in FIG. 1, two silicon wafers, namely a base wafer 1 to be a base and a bond wafer 2 to be an SOI layer which are suitable for device specifications are prepared. In this embodiment, an **epitaxial** wafer consisting of a silicon mirror wafer on which an **epitaxial** layer 13 having a thickness of about 10 .mu.m was grown is employed as a bond wafer 2.

Detail Description Paragraph - DETX (5):

[0055] In step (b), at least one of the wafers, the bond wafer (**epitaxial** wafer) 2 in this case is subjected to thermal oxidation so as to form on the surface thereof an oxide film 3 having a thickness of about 0.1 .mu.m to 2.0 .mu.m.

Detail Description Paragraph - DETX (6):

[0056] In step (c), **hydrogen** ions or rare gas ions are **implanted** into one surface, on which the **epitaxial** layer is formed, of the bond wafer 2 on which oxide film is formed, in order to form a fine bubble layer (enclosed layer) 4 which extends in parallel to the surface at a position corresponding to the mean penetration depth of ion **implantation**. The implantation temperature is preferably 25-450.degree. C.

Detail Description Paragraph - DETX (7):

[0057] In step (d), the base wafer 1 is superposed on the **hydrogen** ion-**implanted** surface (the **epitaxial** layer formed surface) of the **hydrogen** ion-**implanted** bond wafer 2 via the oxide film, and they are brought in close contact with each other. When the surfaces of the two wafers are brought into contact with each other at ambient temperature in a clean atmosphere, the wafers adhere to each other without use of adhesive or the like.

Detail Description Paragraph - DETX (8):

[0058] In step (e), there is performed a heat treatment for delamination in which a delaminated wafer 5 is delaminated from an SOI wafer 6 (composed of the SOI layer 7, a buried oxide layer 3, and a base wafer 1) while the enclosed layer 4 is used as a delaminating plane. The heat treatment is performed, for example, at a temperature of about 500.degree. C. or higher in an inert gas atmosphere so as to cause crystal rearrangement and bubble cohesion, and thereby the delaminated wafer 5 is delaminated from the SOI wafer 6. In this case all of the SOI layer 7 is made of an **epitaxial** layer.

Detail Description Paragraph - DETX (12):

[0062] The SOI wafer 6 of high quality having the SOI layer 7 consisting of an **epitaxial** layer of high crystal quality and high thickness uniformity can be

produced (step (h)) through the steps described above.

Detail Description Paragraph - DETX (13):

[0063] In the above hydrogen ion delaminating method, the delaminated wafer 5 is produced as a by-product in the step (e) of FIG. 1. The thickness of the SOI layer produced by the hydrogen ion delaminating method is generally 0.1 to 1.5 microns, and 2 microns at the thickest. Accordingly, the delaminated wafer 5 has a sufficient thickness. Therefore, production cost for the SOI layer can be significantly reduced by reusing the delaminated wafer as a silicon wafer. Particularly, when the **epitaxial** wafer having the **epitaxial** layer with thickness of about 10 microns is used as a bond wafer as in the above-mentioned embodiment, the **epitaxial** layer with thickness of about 8 microns or more remains after delamination. Accordingly, if it can be used as a bond wafer again, production cost for the SOI wafer wherein the **epitaxial** wafer is used can be significantly reduced.

Detail Description Paragraph - DETX (15):

[0065] Furthermore, the damage layer 12 due to **hydrogen** ion **implantation** remains on the delaminated surface 11 of the delaminated wafer, and the surface roughness is worse than that of a general mirror wafer. Particularly, the surface roughness is locally inferior. Accordingly, when the wafer is subjected to preferential etching such as alkali etching, deep pits are formed therein.

Detail Description Paragraph - DETX (16):

[0066] In that case, it would be conceived that all of the peripheral step, the damage layer and the surface roughness is removed by grinding and polishing. However, stock removal will be too much, and processing time will be too long in such a method. Furthermore, in the case that the **epitaxial** wafer is used as a bond wafer as in the above-mentioned embodiment, the **epitaxial** layer will be completely removed, and therefore it will not be able to be reused as an SOI layer.

Detail Description Paragraph - DETX (18):

[0068] In particular, the inventors studied a method wherein a stock removal for reprocessing a delaminated wafer is reduced in order to reprocess and to reuse an expensive wafer with high quality, such as the above-mentioned **epitaxial** wafer, many times.

Detail Description Paragraph - DETX (44):

[0094] There can be thus obtained the recycled (reclaimed) afer wherein the peripheral step of the delaminated wafer and the damage layer due to **hydrogen**

ion **implantation** on the delaminated surface can be removed, and the surface roughness of the delaminated surface can be improved, so that the surface thereof is not inferior to that of the general mirror wafer.

Detail Description Paragraph - DETX (46):

[0096] Namely, for example, when the SOI wafer is produced by the hydrogen ion delaminating method using the **epitaxial** wafer as a bond wafer, and the delaminated wafer produced as a by-product is reprocessed according to the present invention to reproduce an **epitaxial** wafer, the **epitaxial** wafer thus obtained can be reused as a bond wafer, so that the **epitaxial** layer of the expensive **epitaxial** wafer can be reprocessed many times to be reused as a SOI layer. Accordingly, a SOI wafer having high quality can be obtained at low cost.

Detail Description Paragraph - DETX (50):

[0100] Particularly, when the **epitaxial** wafer is used as a bond wafer, the resultant delaminated wafer can also be used as a general **epitaxial** wafer.

Detail Description Paragraph - DETX (54):

[0102] Two silicon mirror wafers having resistivity of 1.0 to 2.0 .OMEGA..multidot.cm and a diameter of 150 mm wherein a conductive type is p type were prepared. As for one of these wafers, an **epitaxial** layer having a thickness of about 10 microns was grown. The **epitaxial** wafer was used as a bond wafer, and processed through steps (a) to (h) shown in FIG. 1 according to the hydrogen ion delaminating method to fabricate SOI wafers. Thickness of SOI layer was 0.2 micron. The major process conditions used in the method were as follows.

Detail Description Paragraph - DETX (56):

[0104] 2) Conditions of **hydrogen implantation**: H.sup.+ ions, **implantation** energy of 69 kev, **implantation** dose of 5.5.times.10.sup.16/cm.sup.2;

Detail Description Paragraph - DETX (59):

[0107] The high quality SOI wafer having the SOI layer of the **epitaxial** layer with thickness of 0.2 micron could be thus obtained, and the delaminated wafer 5 was also produced as a by-product in step (e) of FIG. 1.

Detail Description Paragraph - DETX (66):

[0114] As shown in FIG. 5, it is apparent that a damage layer having a depth of about 100 nm exists on the surface of the delaminated wafer. OSFs observed in a position deeper than 100 nm were likely generated as a result that nuclei of OSF was formed in the **epitaxial** layer due to crystal defects which have been

originally present in the substrate itself.

Detail Description Paragraph - DETX (77):

[0125] After the heat treatment with rapid heating/rapid cooling apparatus, OSF density on the surface as measured by subjecting the wafer to oxidation and preferential etching and being observed with a microscope was about 10 numbers/cm.sup.2, which is equivalent to the density of OSF generated in an **epitaxial** layer due to influence of the substrate.

Detail Description Paragraph - DETX (78):

[0126] As described above, the delaminated wafer reprocessed according to the present invention has a quality good enough for reuse as an **epitaxial** wafer again.

Detail Description Paragraph - DETX (79):

[0127] Accordingly, the reprocessed delaminated wafer was used as a bond wafer as shown in FIG. 2(F). Namely, the above-mentioned recycle (reclaimed) wafer was used as a bond wafer 2 in FIG. 1(a). As the delaminated wafer was made only 1 micron thinner by being polished to remove a peripheral step, it still has a thickness of about 9 microns. Then, the steps shown in FIG. 1 was performed to prepare SOI wafer in accordance with hydrogen ion delaminating method. High quality SOI wafer wherein SOI layer consists of the **epitaxial** layer could be obtained without any problems.

Claims Text - CLTX (3):

2. A method of recycling a delaminated wafer produced as a by-product in producing an SOI wafer according to a hydrogen ion delaminating method in which an **epitaxial** wafer is used as a bond wafer by reprocessing it for reuse as a silicon wafer, wherein at least polishing of the delaminated wafer for removing of a step in the peripheral part of the delaminated wafer and heat treatment in a reducing atmosphere containing hydrogen are conducted as the reprocessing.